AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-8. (Canceled)

9. (New) An integrated circuit comprising a microprocessor and a set of peripheral devices including at least one communication interface for external access, wherein said peripherals, unlike said communication interface, are connected to said microprocessor by an interconnection bus on which the data length is equal to the standard data length of the data processed by said microprocessor, said integrated circuit also comprising a security module connected to said interconnection bus and to said communication interface by a dedicated link,

wherein the length of the data processed by the security module is greater than the standard data length of the data processed by the microprocessor, and the integrated circuit further comprises means for adapting the length of the data processed by the security module to the standard data length.

10. (New) A circuit according to claim 9, wherein said means for adapting the length of the data processed by the security module to the standard data length includes a cache memory, associated with the microprocessor and provided with a cache memory controller which, upon accessing the cache memory, causes it to transmit to the security module data having a length equal to the standard data

length, whereby the processing of the data by the security module is performed on the fly.

11. (New) A circuit according to claim 10, wherein, during the ciphering of the data by the security module, the cache memory prepares data having a length greater than the standard data length, whereby said data can be accepted at the input of the security module.

12. (New) A circuit according to claim 11, wherein, during the deciphering of the data by the security module, the cache memory breaks the deciphered data available at the output of the security module, which has a length greater than the standard data length, into standard-length data.

13. (New) A circuit according to claim 12, wherein the security module uses a secret key algorithm which processes data having a length of at least 64 bits, and wherein the standard length of the data processed by the microprocessor is less than 64 bits.

14. (New) A circuit according to claim 13, wherein said secret key algorithm is the AES algorithm.